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**PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Attn: OIPE

Hiroyoshi TOMINAGA et al.

Application No.: 10/500,278

Docket No.: 120214

Filed: June 29, 2004

For: WAFER DOUBLE-SIDE POLISHING APPARATUS AND DOUBLE-SIDE  
POLISHING METHOD

**REQUEST FOR CORRECTION OF PALM RECORDS**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Attached is a photocopy of the original filing receipt on which errors have been corrected in red. These errors are being brought to the attention of the Patent and Trademark Office so that it may correct its records.

Respectfully submitted,

William P. Berridge  
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WPB:JOC/mlo

Date: March 2, 2005

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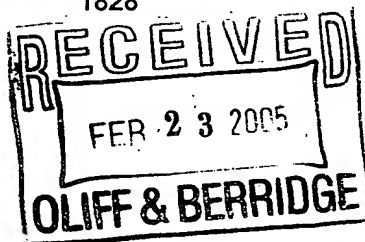
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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/500,278	06/29/2004	3723	1828	120214	10	37	10

25944  
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CONFIRMATION NO. 9347

## FILING RECEIPT



\*OC000000015193300\*

Date Mailed: 02/17/2005

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### Domestic Priority data as claimed by applicant

This application is a 371 of PCT/JP03/03743 03/26/2003

### Foreign Applications

JAPAN 2002-91087 03/28/2002  
JAPAN 2002-91207 03/28/2002

Projected Publication Date: 05/26/2005

Non-Publication Request: No

Early Publication Request: No

Title wafer double - side polishing  
~~Double side polishing device for wafer and double side polishing method~~  
apparatus and double-side polishing  
Preliminary Class method  
451

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